

**THAT WHICH IS CLAIMED IS:**

1. A data transceiving station of digital data frames comprising a digital modem (MODEM) coupled to a transmission line, a microprocessor ( $\mu$ P) receiving demodulated data from said modem according to a Packet Mode or a Bit Mode transmission, an interface circuit (SERIAL\_INTERFACE) between said microprocessor ( $\mu$ P) and said digital modem (MODEM) characterized in that  
said interface circuit (SERIAL\_INTERFACE)  
switches from a Packet Mode to a Bit Mode transmission and/or viceversa during transfer of a data frame to said microprocessor.
2. The data transceiving station of claim 1, wherein said transmission line is a line of an electric power distribution network and said modem (MODEM) generates an information on the detection of an energy level greater than a pre-established threshold in a frequency band selected for transmission over said line.
3. The data transceiving station of claim 2, characterized in that it comprises a circuit (ZC) detecting the zero-crosses of the network voltage and producing a logic signal (ZCOUT) that is also input to said modem (MODEM).
4. A monolithically integrated multichannel transceiver of digital frames over a line of an electric distribution power network, comprising a modem (MODEM) having a register for data storage (CONTROL\_REGISTER) and means for controlling their integrity and signalling any eventual corruption of at least one bit, a serial interface (SERIAL\_INTERFACE),

including a receiving section (RX\_SECTION) and a transmitting section (TX\_SECTION), coupling said modem to the external world, an oscillator (OSCILLATOR) generating carrier frequencies fed to said modem, a power interface circuit (PLI), coupled to said modem and driving an external coupling circuit to said line, characterized in that it comprises

15           a circuit (ZC) detecting the zero-crosses of the network voltage and producing an output logic signal (ZCOUT) coupled to an input of said modem (MODEM) and to a pin of the transceiver;

20           said modem detecting the energy level in a certain frequency band selected for transmission over said line, producing a logic signal on a dedicated pin (BU) when said energy level surpasses a pre-established threshold;

25           said transmitting section (TX\_SECTION) of the serial interface (SERIAL\_INTERFACE) comprises a logic processing circuit (BUFFER\_CONTROL\_UNIT) and a work memory (BUFFER) for organizing a demodulated bit stream (RECOVERED\_DATA) coming from the modem in a stream (BC) of data structured in packets, a multiplexer (MULTIPLEXER)

30           receiving on a first input said demodulated bit stream (RECOVERED\_DATA) and said stream of structured data (BC) and operating a selection between said two streams outputting (DATA\_OUT) either a not structured Bit Mode bit stream or a Packet Mode data stream organized in

35           packets, in function of a selection signal (BURST\_ENABLE) and a control unit (SERIAL\_INTERFACE\_CONTROL\_UNIT) producing said selection signal (BURST\_ENABLE) and a clock signal (RECOVERED\_CLOCK) of said input bit stream (RECOVERED\_DATA).

5.       The transceiver of claim 4 wherein  
said logic circuit processing  
(BUFFER\_CONTROL\_UNIT) produces a third clock signal (A)

G E N E R A T E D   B Y   C O M P U T E R

constituted by sequences of N pulses of a second clock  
5 signal (BURST\_CLOCK) having frequency multiple of the  
frequency of said clock signal (RECOVERED\_CLOCK) of the  
input bit stream at pre-established intervals;

said multiplexer (MULTIPLEXER) receives said  
clock signal (RECOVERED\_CLOCK) of the input bit stream  
10 (RECOVERED\_DATA) and said third clock signal (A),  
outputting a fourth clock signal (CLR/T) equal to said  
third clock signal (A) or to said first clock signal  
(RECOVERED\_CLOCK) depending on whether said selection  
signal (BURST\_ENABLE) selects said not structured bit  
15 stream (RECOVERED\_DATA) or said data flow structured in  
packets (BC).

6. The transceiver of claim 4 wherein  
said work memory (BUFFER) comprises  
a first register (SHIFT\_REGISTER\_1) and second  
register (SHIFT\_REGISTER\_2) fed with said demodulated  
5 datastream (RECOVERED\_DATA), and clocked with respective  
clock signals (Z1, Z2), and outputting a first data  
signal (S1) and a second data signal (S2),  
respectively;  
said logic processing circuit  
10 (BUFFER\_CONTROL\_UNIT) comprises  
a first modulus N counter (COUNTER\_1) fed with  
said first clock signal (RECOVERED\_CLOCK) producing a  
first end-computation signal (C1) when N pulses have  
been counted,  
15 a second modulus N counter (COUNTER\_2) fed  
with said second clock signal (BURST\_CLOCK) and enabled  
by said first end-computation signal (C1), producing a  
second end-computation signal (C2) that is enabled by  
said first end-computation signal (C1) and disabled  
20 when said second counter (COUNTER\_2) counts N pulses of  
said second clock signal (BURST\_CLOCK),

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a second multiplexer (MUX\_1) and third multiplexer (MUX\_2) fed with said demodulated bit stream (RECOVERED\_DATA) and with said third clock signal

25 (A) producing respectively said clock signals (Z1, Z2) corresponding alternately to said third clock signal (A) and to said first clock signal (RECOVERED\_CLOCK), depending on a switching signal (T), that toggles every N pulses of said first clock signal;

30 a logic AND gate, combining said second clock signal (BURST\_CLOCK) and said second end-computation signal (C2), producing said third clock signal (A) as periodic sequences of N pulses of said second clock signal (BURST\_CLOCK) output at each enablement of said

35 first end-computation signal (C1),

a fourth multiplexer (MUX\_3) fed with said first data signal (S1) and with said second data signal (S2) and outputting a third data signal (BC) corresponding to said first data signal (S1) or to said

40 second data signal (S2) depending on said switching signal (T).

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